taper. Conventional machining of the taper may be impractical, but other techniques can be devised. It is, however, emphasized that the transition described here was not intended for production but for a specific measurement program [16].

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A Low-Noise GaAs Monolithic Broad-Band Amplifier Using a Drain Current Saving Technique

K. OSAFUNE, N. KATO, T. SUGETA, AND Y. YAMAO

Abstract—**A low-noise and low-power GaAs monolithic broad-band amplifier is proposed and has been developed, which has a new cascade connection with a large gate-width input FET and the other circuits in such a way that the output stage current flows through the input FET. The fabricated amplifier operates on +5-V single supply voltage, and provides a 3.3-dB noise figure, less than 180-mW power dissipation, and a 10-MHz–2.0-GHz bandwidth with 16-dB gain.**

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I. INTRODUCTION

Recent advances in GaAs IC technology make it possible to develop GaAs monolithic broad-band amplifiers for mobile radio applications. For these amplifiers, both a low dc power dissipation and a low noise figure are required. From a practical point of view, single-power supply operation and good input/output matching are desirable. To meet these needs, low-noise, low power-dissipation GaAs monolithic broad-band amplifiers were developed [1]–[3]. They achieved a low noise figure and good input/output matching by using RC parallel feedback, and also achieved low power dissipation by using inductive loads (choke coils). Although inductive loads are effective in reducing amplifier power dissipation, choke coil sizes are almost 10 times as large as IC chips below the S-band.

In this short paper, we propose a new circuit construction which enables both power saving and low-noise operation in the monolithic GaAs amplifier for VHF–UHF mobile radio systems. Design considerations and performance characteristics of this amplifier are described as follows.

II. CIRCUIT DESIGN

In order to construct a low-noise amplifier, it is desirable to increase the input-stage FET transconductance g_m. Therefore, the input-stage FET must have a wide gate width to afford high g_m. To make input matching, a resistor negative feedback circuit is advantageous from the view point of low-noise characteristics. Furthermore, if the amplifier open-loop gain is high, the feedback resistor can be increased, and the noise generated from the feedback resistor can be suppressed. For increasing the open-loop gain, multistage construction is effective [2]. But dc drain current also increases as the number of the stages increases. If we can get high gain without a drain current increase, both a low noise figure and low power dissipation are possible.

For this purpose, a new circuit construction amplifier (shown in Fig. 1) has been developed. This amplifier consists of three stages; the input stage ($Q1, Q2$) and two source follower stages ($Q3, Q4$ and $Q5, Q6$). The input stage owns a wide-gate input FET $Q1$ and a relatively high-impedance resistor load R_d to obtain both a low noise figure and high gain. The amplifier open-loop gain is mainly determined by this stage. The two source follower stages do not amplify signal voltages, but they do lower the amplifier output impedance to 50 Ω. The small input capacitance of the intermediate source follower FET $Q3$ makes it possible to increase the resistor load R_d without decreasing the amplifier bandwidth; thus, the open-loop gain increases as well. The output matching is performed by determining the transconductance of the output FET $Q5$ equal to 20 mS ($=1/50$ Ω). A negative feedback circuit (R_f, C_f) is used for input matching with little influence on the noise figure. The gate-grounded FET $Q2$ is used to make the input FET drain voltage constant and yields bias voltages of current source FET's $Q4$ and $Q6$.

In this construction, the bias currents of two source follower stages pass through $Q1$. Therefore, the amplifier's total drain current is equal to that of the input FET $Q1$. Due to the adoption of this multistage cascade construction, high gain and a low noise figure are attained without an increase in current.

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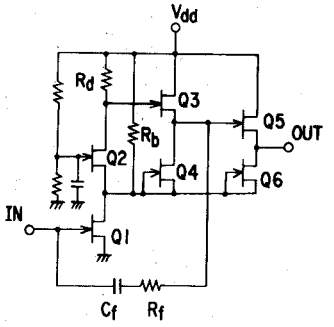

Fig. 1. Schematic diagram for a newly developed GaAs monolithic amplifier. R_f: Feedback resistor.

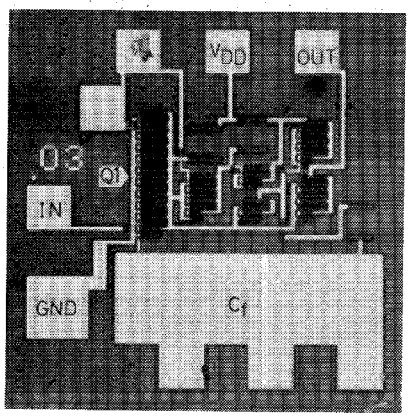

Fig. 2. Microphotograph of the fabricated amplifier.

TABLE I
DESIGN PARAMETERS OF THE AMPLIFIER
W_g: GATE-WIDTH.

W_g	Q1	540 μm
	Q2	170
	Q3	85
	Q4	85
	Q5	170
	Q6	170
Rd		600 Ω
Rb		530
Rf		1200
Cf		17pF

The amplifiers' design parameters are shown in Table I. Gate length and threshold voltage for the FET's used are 0.7 μm and −1 V, respectively. The intermediate source follower FET $Q3$ gate width is determined by circuit simulations for the amplifier bandwidth to be as broad as possible.

Scattering parameters and the noise figure are calculated by circuit simulation programs ASTAP and SPICE with the FET model described in [4] and [5].

III. FABRICATION

The amplifiers were fabricated by the self-aligned implantation for n^+-layer technology (SAINT) [6] process. Active layers for the FET's and the low sheet-resistive layers (500 Ω/square) for resistors were formed by two ion implantations into a 2-in LEC wafer. The capacitors are MIM-type, where the dielectric material is PCVD-SiN. Details of the other processes are described in [7].

A microphotograph of the fabricated amplifier chip is shown in Fig. 2. The gate finger width for the FET's and the space between the electrode for resistors were both 50 μm. Chip size was 0.8 × 0.8 mm square.

IV. PERFORMANCE

The amplifiers were mounted on 50-Ω coplanar test fixtures and their characteristics were measured by an automatic network analyzer (HP-8545A) and an automatic noise-figure meter (AIL-75).

Frequency dependences for transducer gain S_{21} and noise figure NF for the amplifier are shown in Fig. 3. The amplifier had a 16-dB flat gain and a 2-GHz, 3-dB bandwidth under a power dissipation of 180 mW ($V_{dd} = +5$ V). The calculated frequency dependences for transducer gain S_{21} are shown by the solid line

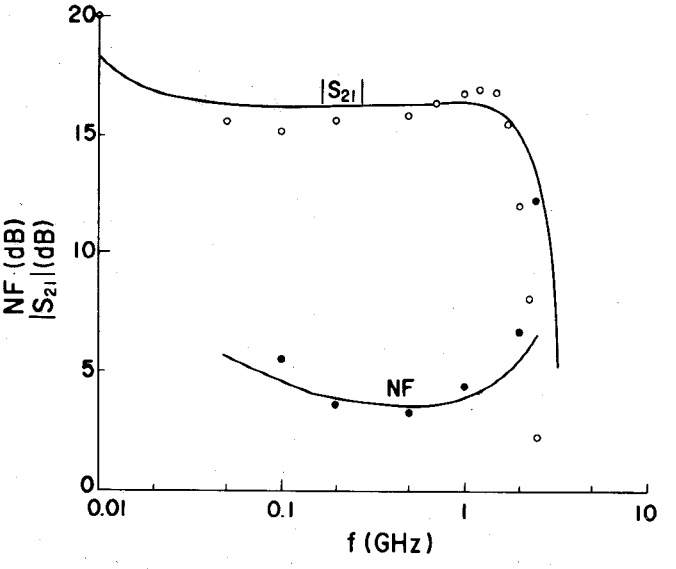

Fig. 3. The frequency dependences of the transducer gain S_{21} and noise figure for the amplifier. Points show measured values. Solid lines indicate the calculated frequency dependences of S_{21} and NF.

in Fig. 3. In this computer simulation, the average value of transconductance (110 mS/mm at $V_{ds} = 1.5$ V and $V_{gs} = 0$ V) for the fabricated FET was used. Drain conductance and parastic capacitances were considered to obtain the best fitting. The amplifier had a 3.3-dB noise figure NF at approximately 1 GHz. Fig. 3 also shows the computed frequency dependences for the noise figure using the modified SPICE simulation program for a GaAs FET, assuming that $P = 2$, where P is the well-known factor in the expression for the drain current noise defined by $i_{dn} = 4kT\Delta f g_m P$.

The amplifier developed here is briefly compared to recently reported GaAs monolithic amplifiers. The noise figure of the amplifier is much lower than that of a common gate-type monolithic amplifier [8]. The power dissipation of the amplifier is sufficiently lower than that of common source-type amplifiers with resistive feedback [9]–[11], though the noise figure is slightly higher than that of those amplifiers.

V. CONCLUSION

A low-noise, low power-dissipation GaAs monolithic broadband amplifier has been developed for VHF–UHF mobile radio systems. The amplifier operates with a single power supply, requires no external choke coils, provides a 3.3-dB noise figure

with less than 180-mW dc power dissipation, and has a 10-MHz–2.0-GHz bandwidth with 16-dB gain. It has been concluded that the new circuit construction is effective for low-noise, low power-dissipation GaAs monolithic amplifiers. This amplifier is capable for use in mobile radio systems.

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Polygonal Coaxial Line with Round Center Conductor

WEIGAN LIN

***Abstract*—The complex potential function $W = A(\ln z + C_N z^N)$ generates a zero-potential line approximating a regular polygon of N sides very closely, except in the nearly field-free region. By means of this function we work out the characteristic impedance, the power-carrying capacity, and the attenuation constant of the polygonal line of N sides with a round inner coaxial conductor in a closed form of elementary functions with good accuracy compared to more complex solutions.**

Results for $N = 3$ are believed to be nearly as good as those available in the literature.

I. INTRODUCTION

Considerable work has been done on transmission lines in which the two conductors are not members of the same orthogonal cylindrical coordinate system. These are difficult electrostatic problems, one of which is the well-known charged sphere in a cylinder [1]. Riblet solved the characteristic impedance of a TEM coaxial line with a round inner and square outer conductor (shown in Fig. 1) and also of the related transmission line of a square inner and round outer conductor by means of a well-known transformation, work that first appeared in 1935 [2]. Subsequent work appeared in 1982 on this same problem [3], [7]. The purpose of this paper is to investigate the characteristics of the coaxial line with a round inner conductor of radius a and a polygonal outer conductor of N sides with an inscribed circle of radius b, as shown in Fig. 2. In comparison with the existing data, all our results are in closed forms, in elementary functions, and have accuracy nearly as good as data available in the literature, but the simplicity in the Z_0 formula surpasses all of them except for $N = 4$. The forms of our results allow us to calculate the power-carrying capacity and the attenuation constant of the line.

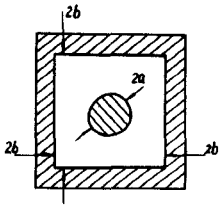

Fig. 1. TEM coaxial line with round inner and square outer conductor.

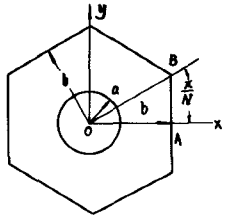

Fig. 2. TEM coaxial line with polygonal outer conductor of N sides and round inner conductor.

II. THE METHOD

We generalize Schelkunoff's work on the TEM transmission line with a round inner conductor and square outer conductor [4] by the following complex potential function:

$$W = U + jV = A\left[\ln\frac{z}{R} + C_N\left(\frac{z}{R}\right)^N\right] \tag{1a}$$

with

$$U = A\left[\ln\frac{\rho}{R} + C_N\left(\frac{\rho}{R}\right)^N \cos N\varphi\right] \tag{1b}$$

$$V = A\left[\varphi + C_N\left(\frac{\rho}{R}\right)^N \sin N\varphi\right] \tag{1c}$$

where (ρ, φ) are the polar coordinates, and A, R, and C_N are constants to be determined to fit the boundary conditions of the coaxial line of Fig. 2. If U and V are, respectively, the potential and the flux function, it follows that the charge per unit length Q of this coaxial line is

$$Q = \epsilon[V] = 2\pi\epsilon A. \tag{2}$$

Now C_N is nonzero, so the zero-potential line is determined by the following equation from (1b):

$$-C_N \cos N\varphi = \left(\frac{\rho}{R}\right)^{-N} \ln\frac{\rho}{R}. \tag{3}$$

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